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10/635,198	08/06/2003	Rolf Harjung	US 20 02 1052-2	8328

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EXAMINER	
ORTIZ RODRIGUEZ, CARLOS R	
ART UNIT	**PAPER NUMBER**
2125	
MAIL DATE	**DELIVERY MODE**
05/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/635,198	HARJUNG, ROLF	
	Examiner	Art Unit	
	Carlos Ortiz-Rodriguez	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-11 and 13-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-11 and 13-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/20/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. It should be noted that during a telephone conversation the examiner identified possible 35 USC 101 rejections. Applicant's representative proposed amendments to said claims. Said amendments are acceptable.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-11 rejected under 35 U.S.C 112, second paragraph. The term "substantially" in claims 1, 6 and 9 is a relative term which renders the claim indefinite. The term "substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

4. Claims 1-11 rejected under 35 U.S.C 112, second paragraph. The term "each section" (Claim 1, L12) and the term "the slope" (Claim 1, L20) renders the claim indefinite. There is insufficient antecedent basis for these limitations in the claim.

5. Claims 6 and 7 rejected under 35 U.S.C 112, second paragraph. The term "the real step signal" (Claim 6, L3-4) renders the claim indefinite. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 14 and 17 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. According to the preamble, the claim seems to be system claim however the body of the claim are steps of a method.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claim 13-17 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claim language is directed towards software per se.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-3, 6-9, 11 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forster U.S. Patent No. 3,393,363 in view of Moriyasu et al. U.S. Patent No. 5,349,539.

Regarding claims 1 and 3 and 11, 13-16, Forster discloses a method comprising:

(a) receiving a measured electrical signal response (input signal source) in at least one of time domain or frequency domain (C1 L56-60),

(b) sampling (triangular scan signal) the received measured electrical signal response at a plurality of sampling points (repetition rate/ sampling periods) and approximating (output from encoder) each section of the received measured electrical signal response between two adjacent sampling points by a respective linear curve section (C5 L8-36 and Fig 30b):

(c) for each section of the measured electrical signal response: (i)selecting a pulse unit for generating a pulse having a transition between the two adjacent sampling points associated with the section and (C5 L6-9) (ii) selecting a current source or a voltage source (Fig 8, elements 81 and 82, C9 L31-44) providing, in response to the pulse from the selected pulse unit, an output signal (output from element 19) corresponding to the slope of the section;

(d) selecting an integrating unit for superimposing (element 13 and 16) the output signals from each of the selected current or voltage sources for generating an approximated signal response: and

(e) creating a model based on the selected pulse units, the selected current or voltage sources and the selected integrating unit (Fig 30b).

But Forster fails to clearly specify that the measured electrical signal response substantially represents an electrical behavior of an electronic device (C3 L13-18).

However, Forster in combination with Moriyasu disclose that the measured electrical signal response substantially represents an electrical behavior of an electronic device (Moriyasu, C3 L13-18).

Therefore at time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the above invention suggested by Forster and combining it with the invention disclosed by Moriyasu. The results of this combination would lead to modeling an electronic device.

One of ordinary skill in the art would have been motivated to do this modification because in this art it is the electrical behavior of an electronic device is obtained by providing a stimulus as suggested by Moriyasu.

Regarding claim 2 the combination of Forster and Moriyasu disclose all the limitations of the base claims as outlined above. Furthermore, Forster in combination with Moriyasu disclose that the measured electrical signal response comprises a signal selected from the group consisting of: a measured signal response to a predetermined electrical signal provided as a stimulus signal to the electronic device, and a response, to a step signal so that the measured signal response comprises a step response (Moriyasu C3 L13-18, Fig 5-8 and Claim 1).

Regarding claim 6 the combination of Forster and Moriyasu disclose all the limitations of the base claims as outlined above. Furthermore, Forster in combination with Moriyasu disclose calculating a substantially ideal step response from a measured real step signal having a finite

slew rate and from the measured electrical signal response to the real step signal (Forster, Fig 2a).

Regarding claim 7 the combination of Forster and Moriyasu disclose all the limitations of the base claims as outlined above. Furthermore, Forster in combination with Moriyasu disclose that the ideal step response is calculated by a technique selected from the group consisting of a Fourier Transformation and a Fast Fourier Transformation (Moriyasu C6 L31-42).

Regarding claim 8 the combination of Forster and Moriyasu disclose all the limitations of the base claims as outlined above. Furthermore, Forster in combination with Moriyasu disclose that the model of the electronic device is generated by a system selected from the group consisting of a simulation system and a SPICE simulation system (Moriyasu C1 L9-20 and C4 L10-42).

Regarding claim 9 and 17 the combination of Forster and Moriyasu disclose all the limitations of the base claims as outlined above. Furthermore, Forster in combination with Moriyasu disclose that the electronic device is selected from the group consisting of: a substantially linear device, a substantially time-invariant device, an electrical device, a signal path, a high-speed signal path, a line drive output, a line drive output of an automated test equipment, and an n-port network (Moriyasu C3 L13-18).

11. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Forster U.S. Patent No. 3,393,363 in view of Moriyasu et al. U.S. Patent No. 5,349,539 and in view of Marzalek et al. U.S. Patent No. 5,162,723.

Regarding claim 10 the combination of Forster and Moriyasu disclose all the limitations of the base claims as outlined above.

But Forster in combination with Moriyasu fails to clearly specify that the measured electrical signal response of the electronic device is a measurement selected from the group consisting of a time domain reflection measurement and a time domain transmission measurement.

However, Forster in combination with Moriyasu and Marzalek et al. disclose that the measured electrical signal response of the electronic device is a measurement selected from the group consisting of a time domain reflection measurement and a time domain transmission measurement (Marzalek, C26 L28-32) .

Therefore at time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the above invention suggested by Forster in combination with Moriyasu and combining it with the invention disclosed by Marzalek.

One of ordinary skill in the art would have been motivated to do this modification because in this art reflection measurements are frequently necessary as suggested by Marzalek et al.

Citation of Pertinent Prior Art

12. The following prior art made of record is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to modeling and electronic device:

a. U.S. Patent No. 3,431,490 to Kwap et al., which discloses apparatus for indicating response of a test circuit to an applied pulse.

b. U.S. Patent No. 4,438,404 to Philipp, which discloses signal sampling system.

c. U.S. Patent No. 5,343,405 to Kucera et al., which discloses automatic extraction of pulse-parameters from multi-valued functions.

d. U.S. Patent No. 5,793,801 to Fertner et al. which discloses frequency domain signal reconstruction compensating.

e. U.S. Patent No. 5,799,172 to Gullapalli et al., which discloses method of simulating an integrated circuit.

f. U.S. Patent No. 5,886,586 to Lai et al., which discloses general constant frequency pulse-width modulators.

g. U.S. Patent No. 6,653,848 to Adamian et al. which discloses method and apparatus for linear characterization of multi-terminal single-ended or balanced devices.

h. U.S. Patent No. 6,836,574 to Shioda et al., which discloses optical domain optical signal sampling device.

i. U.S. Patent No. 6,856,148 to Bodenstab, which discloses method and program product for evaluating a circuit.

The following publications are cited to further show the state of the art with respect to modeling an electronic device:

j. U.S. Pub. No. 2003/0071606 to Sunter, which discloses method and circuit for testing high frequency mixed signal circuits with low frequency signals.

k. U.S. Pub. No. 2004/0096021 to Koval, which discloses communications methods for narrow band demodulation.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carlos Ortiz-Rodriguez **(new examiner of record)** whose telephone number is **571-272-3677.**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Carlos Ortiz-Rodriguez
Patent Examiner
Art Unit 2125

April 30, 2007

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